ACADEMIC LESSON PLAN FOR WINTER -2023

Dept. of Electronics & Telecommunication, RKCAT Polytechnic,

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VLSI & EMBEDDED SYSTEM **(TH-2)**

PERIOD	TOPIC COVERED	DATE	REMARKS
UNIT-01 TOTAL PERIOD-12 Introduction to VLSI & MOS Transistor 1ST	Historical perspective- Introduction		
2ND	Classification of CMOS digital circuit types		
3RD	Introduction to MOS Transistor& Basic operation of MOSFET.		
4TH	Structure and operation of MOSFET (n-MOS enhancement type) & COMS MOSFET V-I characteristics,		
5TH	Working of MOSFET capacitanc		
6TH	Modelling of MOS Transistors including Basic concept the		
7TH	SPICE level-1 models, the level-2and level-3 model		
8TH	. Flow Circuit design procedures		
9TH	VLSI Design Flow & Y chart		
10TH	VLSI Design Flow & Y chart		
11TH	Full custom Design Hierarchy		

12TH	VLSI design styles-FPGA, Gate Array Design, Standard cells based		
UNIT-2 Total- 10 1st	Simplified process sequence for fabrication		
2ND	Basic steps in Fabrication processes Flow		
3RD	Fabrication process of nMOS Transistor		
4TH	CMOS n-well Fabrication Process Flow		
5TH	MOS Fabrication process by n-well on p-substrate		
6TH	CMOS Fabrication process by P-well on n-substrate		
7TH	Layout Design rules		
8TH	Stick Diagrams of CMOS inverter		
9TH	Stick Diagrams of CMOS inverter		
10TH	Stick Diagrams of CMOS inverter		
Unit-03 MOS Inverter 1ST&2ND **TOTAL-09**	Basic nMOS inverters,		
3RD&4TH	Working of Resistive-load Inverter		
5TH &6TH	Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter CMOS Inventor design with delay constraints –		
7TH &8TH	CMOS inverter – circuit operation and characteristics and interconnect effects: Delay timedefinitions		
9TH	Two sample mask lay out for p-type substrate		

Unit-4: TOTAL-15 1ST &2ND ,3RD	Define Static Combinational logic ,working of Static CMOS logic circuits (Two-inputNAND Gate) CMOS logic circuits (NAND2 Gate)		
4TH &5TH &6TH	CMOS Transmission Gates(Pass gate) Complex Logic Circuits – Basics Classification of Logic circuits based on their temporal behavior		
7TH &8TH &9TH	SR Flip latch Circuit, Clocked SR latch only. CMOS D latch		
9TH &10TH &11TH	Basic principles of Dynamic Pass Transistor Circuits		
12TH &13TH &15TH	Dynamic RAM, SRAM, Flash memory		
Unit-5: System Design method & synthesis TOTAL-05 1ST &2ND	Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xlinx		
3RD &4THND	Design strategies & concept of FPGA with standard cell based design		
5TH	VHDL for design synthesis using CPLD or FPGA Raspberry Pi - Basic idea		
Unit-6 TOTAL-10 1ST &2ND	Embedded Systems Overview, list of embedded systems,characteristics ,example – A DigitalCamera Embedded Systems Technologies--Technology – Definition Technology for Embedded Systems -Processor Technology -IC Technology		

3RD &4THND	Design Technology-Processor Technology, General Purpose Processors – Software,Basic Architecture of Single Purpose Processors – Hardware		
5TH&6TH	IC Technology- Full Custom / VLSI,Semi-Custom ASIC (Gate Array & Standard Cell),		
7TH&8 TH	PLD(Programmable Logic Device) Basic idea of Arduino micro controller		
9th &10th	Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)		

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